Mehrdad Reshadi

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Work Experience

Principal Software Engineer / Architect   02/2013 – present

Instart Logic Inc., 450 Lambert Avenue, Palo Alto, CA 94306.

- Designed, developed, and led a new platform that would allow content transformations run on both client (browser) and server (nodejs) seamlessly and with minimal development effort.
  - Led development of several features based on this new platform including:
    - Client-security based on novel techniques of confinement in the browser
    - Ad-integrity to protect ads on the page from tampering.
- Designed and developed a typed DSL configuration and accompanied services to manage, optimize, and deliver configuration of client and micro services in the system. This is now a key component for managing the complexity of Instart services, features, and platforms.
- One of main contributors in the design and development of optimization features such as:
  - Html-streaming: partial caching and fast delivery of non-cacheable and dynamic html based on learning.
  - JavaScript-streaming: ship only used part of code based on application profiling and machine learning.
  - Image-streaming: improve user experience by partial delivery of images and delayed back-filling.
- Designed and developed Nanovisor, an in-browser virtualization platform that became the basis of all Instart client-cloud features.
- Created the full stack build system to create and optimize both client (browser) and server (nodejs) code from exact same code base
- Championed and led a multi-repository, component-based CI/CD system to properly test server and client code before release
- Moved all of JavaScript development to TypeScript to improve reliability and productivity.
- Various external public presentations about core features and products.

Senior Staff Engineer   04/2012 – 02/2013

Qualcomm Inc., 3165 Kifer Road, Santa Clara, CA 95051.

- Leading the concurrent JavaScript engine research and development and integrating it with the Zoomm concurrent web browser engine. (https://github.com/reshadi/mcjs)

Staff Engineer   08/2008 – 04/2012

Qualcomm Inc., 3165 Kifer Road, Santa Clara, CA 95051.

- Working on mobile browser performance improvement by enabling concurrency and taking advantage of SoC hardware.
- Developed tool methodologies as part of ESL and Functional Verification CAD groups. Provided training and infrastructure on TLM and SystemC for the engineering teams.
- Designed and developed a framework for generating HDL and C files from IP-XACT register description to be used by verification engineers.

Senior Software Engineer   02/2008 – 08/2008

Synplicity Inc., 600 W. California, Sunnyvale, CA 94086.
(Acquired on May 15, 2008 by Synopsys Inc. 700 East Middlefield Road, Mountain View, CA 94043-4033)

- Developed compilation, optimization, and synthesis algorithms for Verilog and SystemVerilog compilers.

Chief Software Architect   03/1999 – 08/2001

Global Trading Co. (GTC), Fatemi st., Tehran, Iran.

- One of the three key people who analyzed the business process of one of the biggest trading companies in the country. Extracted and formalized the workflow of different departments.
- One of the three key people who designed a complex dynamic web-based collaborative system for automating the business process. The system could follow the individual steps of workflow, ask users to enter data on proper schedules, and produce both detailed and high-level reports. Workflow could be updated in the database.

- Designed and developed an XML-based framework to help web developers program more efficiently. Being done in year 2000, many of the features of my framework were similar to what was later introduced in ASP.NET 2.0 in year 2006.
- Participated in the design of database structure.
- Managed and coordinated several programmers.

Embedded Software Developer   **11/1996 – 03/1999**

Process & Research Co. (PRE), Jordan St., Tehran, Iran.
- Developed several real-time / reliable monitoring and control applications.
- Developed an Axle Test Monitoring System for MEGA Motors Co (An automobile manufacturer).
- Developed a CNC controlling software for a drilling machine in MEGA Motors Co.
- Developed an Engine Test Monitoring System for SANE engine factory.
- Developed a Drilling Machine Controller Software for SANE engine factory.

Patent & Software Release

Patent

1. "*HTML streaming*", US9998521B2, Jun 8, 2015.
2. "*Placeholders for dynamic components in HTML streaming*", US9813480B2, Jan 8, 2015.
3. "*Collection management in document object model virtualization* ", US9953014B1, Nov 8, 2013.
4. "*Smart hierarchical cache using HTML5 storage APIs*", US9531829B1, Nov 1, 2013.
5. "*Pre-processing of scripts in web browsers*", EP2885703B1, Aug 16, 2012.
6. "*Speculative resource prefetching via sandboxed execution*", US9898445B2, Aug 16, 2012.
7. "*On-Line Behavioral Analysis Engine in Mobile Device with Multiple Analyzer Model Providers*", US9747440B2, Aug 15, 2012.
8. "*Html5 i-frame extension*", US9372836B2, March 30, 2012.
9. "*Reducing web browsing overheads with external code certification*", US9819687B2, Jan 26, 2012.
10. "*Encoding labels in values to capture information flows*", US8898780B2, Nov 7, 2011.
11. "*Web browsing enhanced by cloud computing*", US9146909B2, July 27, 2011.
12. "*Hardware support for hashtables in dynamic languages*", US9063749B2, May 27, 2011.
13. "*Concurrent parsing and processing of HTML and JavaScript*", US8413047B2, May 12, 2011.
14. "*Method and apparatus for optimized execution using resource utilization maps*", US9804893B2, Apr 8, 2011.
15. "*Execution of dynamic languages via metadata extraction*", US9003380B2, Jan 12, 2010.
16. "*Retargetable Instruction Set Simulators*", US8621444B2, Jun 1, 2004.

Software Release

- MuscalietJS: An Extensible Portable Layered JavaScript Engine, https://github.com/reshadi/mcjs.
- Mehrdad Reshadi, Bita Gorjiara, "*Web-based NISC tool for custom processor design*", released in September 2005, available at   http://www.cecs.uci.edu/~nisc/
- Mehrdad Reshadi, Bita Gorjiara, "*NISC tool-set for custom processor design*", released in November 2005, available at   http://www.cecs.uci.edu/~nisc/

Education

Ph.D., Information and Computer Sciences   **09/2001 – 12/2007**

University of California, Irvine, Irvine, CA 92697
Advisor: Prof. Daniel Gajski
Dissertation: "No-Instruction-Set-Computer (NISC) Technology Modeling and Compilation"
Contributions:
- Developed the new NISC technology for generating custom processors and dedicated hardware blocks.
- Developed a new cycle-accurate compiler technology that compiles application directly on a datapath without using instruction abstraction. It combines the traditional parallelizing compiler techniques with high-level

synthesis algorithms. This compiler gets a C program (or .NET MSIL assembly) as well as the netlist description of a NISC processor as inputs; and compiles the program directly on the datapath and generates the control bits in every clock cycle. This compiler is used in a design flow for processor customization and C-to-HDL conversion.

- Developed several high-performance retargetable simulation techniques for pipelined processors.
- Developed a new template based instruction-set modeling for developing fast instruction-set simulators.
- Developed a new Petri-net based processor modeling for developing fast cycles-accurate processor simulators.

GPA: 4.00

M.Sc., Computer Engineering   09/1997 – 09/2000
University of Tehran, Tehran, Iran
Advisor: Prof. Zain Navabi
Thesis: "Synthesizable Intermediate Format"
Contributions:
- Developed an object-oriented platform-independent intermediate format for capturing VHDL.
- Developed algorithms for performing logic/RTL synthesis of the captured design in that intermediate format.

Bachelor of Science, Computer Engineering   09/1993 – 09/1997
Sharif University of Technology, Tehran, Iran
Project: "Programmable Function Generator"
Contributions:
- Developed an ISA-Bus card that was installed in a PC and controlled by software to generate sinusoid waveforms with different frequency and amplitude.

Publications

Book Chapter
1. B. Gorjiara, <u>M. Reshadi</u>, D. Gajski, "**Chapter 13: GNR: A Formal Language for Specification, Compilation, and Synthesis of Custom Embedded Processors**", P. Mishra, N. Dutt, *Processor Description Languages: Applications and Methodologies*, Morgan Kaufmann, ISBN: 978-0-1237-4287-2, 2008.
2. B. Gorjiara, <u>M. Reshadi</u>, D. Gajski, "**Chapter 2: Low-Power Design with NISC Technology**", J. Henkel, S. Parameswaran, *Designing Embedded Processors: A Low Power Perspective*, Springer, ISBN: 978-1-4020-5868-4, April 2007.

Journals
1. <u>M. Reshadi</u>, P. Mishra, N. Dutt, "**Hybrid Compiled Simulation: An Efficient Technique for Instruction-Set Architecture Simulation**", *ACM Transactions on Embedded Computing Systems (TECS)*, Volume 8, Issue 3, April 2009.
2. B. Gorjiara, <u>M. Reshadi</u>, D. Gajski, "**Merged Dictionary Code Compression for FPGA Implementation of Custom Microcoded PEs**", *ACM Transactions on Reconfigurable Technology and Systems (TReTS)*, Volume 1, Issue 2, June 2008.
3. <u>M. Reshadi</u>, B. Gorjiara, N. Dutt, "**Generic Processor Modeling for Automatically Generating Very Fast Cycle-Accurate Simulators**", *IEEE Transactions on Computer Aided Design (TCAD)*, Volume 25, Issue 12, pages 2904-2918, December 2006.
4. <u>M. Reshadi</u>, P. Mishra, N. Dutt, "**A Retargetable Framework for Instruction-Set Architecture Simulation**", *ACM Transactions on Embedded Computing Systems (TECS)*, Volume 5, Issue 2, pages 431-452, May 2006.

Conferences
1. P. Ahammad, R. Gaunker, B. Kennedy, <u>M. Reshadi</u>, K. Kumar, A. Pathan, H. Kolam, "**A flexible platform for QoE-driven delivery of image-rich web applications**", IEEE International Conference on Multimedia and Expo 2015, July 2015.
2. A. Anand, M. Reshadi, B. Du, H. Kolam, S. Jaiswal, A. Akella, "**A case for application-managed cache for browser**", IEEE International Conference on Multimedia and Expo 2015, July 2015.

3. B. Robatmili, C. Cascaval, <u>M. Reshadi</u>, M. Kedlaya, S. Fowler, V. Bhavsar, M .Weber, B. Hardekopf, "**MuscalietJS: rethinking layered dynamic web runtimes**", VEE '14 Proceedings of the 10th ACM SIGPLAN/SIGOPS international conference on Virtual execution environments, Pages 77-88, July 2014.

4. M. Kedlaya, J. Roesch, B. Robatmili, <u>M. Reshadi</u>, B. Hardekopf, "**Improved type specialization for dynamic scripting languages**", ACM SIGPLAN Notices, pages 37-48, February 2014.

5. C. Cascaval, S. Fowler, P. Montesinos Ortego, W. Piekarski, <u>M. Reshadi</u>, B .Robatmili, M. Weber, V. Bhavsar, "**ZOOMM: A Parallel Web Browser Engine for Multicore Mobile Devices**", ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), February 2013.

6. <u>M. Reshadi</u>, C. Cascaval, "**Multidimensional dynamic behavior in mobile computing**", 2012 IEEE International Symposium on Workload Characterization (IISWC), pages 113-115, November 2012.

7. <u>M. Reshadi</u>, D. Gajski, "**C-Based Design Flow: A Case Study on G.729a for Voice over Internet Protocol (VoIP)** ", *Design Automation Conference (DAC)*, June 2008.

8. <u>M. Reshadi</u>, D. Gajski, "**Interrupt and Low-level Programming Support for Expanding the Application Domain of Statically-scheduled Horizontally-microcoded Architectures in Embedded Systems**", *Design Automation and Test in Europe (DATE)*, April 2007.

9. B. Gorjiara, <u>M. Reshadi</u>, P. Chandraiah, D. Gajski, "**Generic Netlist Representation for System and PE Level Design Exploration**", *International Symposium on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, October 2006.

10. B. Gorjiara, <u>M. Reshadi</u>, D. Gajski, "**Generic Architecture Description for Retargetable Compilation and Synthesis of Application-Specific Pipelined Datapaths**", *International Conference on Computer Design (ICCD)*, October 2006.

11. J. Trajkovic, <u>M. Reshadi</u>, B. Gorjiara, D. Gajski, "**A Graph Based Algorithm for Data Path Optimization in Custom Processors**",9th *Euromicro Conference on Digital System Design*, September 2006.

12. B. Gorjiara, <u>M. Reshadi</u>, D. Gajski, "**Designing a Custom Architecture for DCT Using NISC Design Flow**", *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Design Contest, 2006.

13. <u>M. Reshadi</u>, B. Gorjiara, D. Gajski, "**Utilizing Horizontal and Vertical Parallelism with No-Instruction-Set Compiler for Custom Datapaths**", *International Conference on Computer Design (ICCD)*, October 2005.

14. <u>M. Reshadi</u>, D. Gajski, "**A Cycle-Accurate Compilation Algorithm for Custom Pipelined Datapaths**", *International Symposium on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, September 2005.

15. <u>M. Reshadi</u>, P. Mishra, "**Memory Access Optimizations in Instruction-Set Simulators**", *International Symposium on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, September 2005.

16. <u>M. Reshadi</u>, N. Dutt, "**Generic Pipelined Processor Modeling and High Performance Cycle-Accurate Simulator Generation**", *Design Automation and Test in Europe (DATE)*, March 2005.

17. B. Gorji-Ara, P. Chou, N. Bagherzadeh, D. Jensen, <u>M. Reshadi</u>, "**Fast and Efficient Voltage Scheduling by Evolutionary Slack Distribution**", *Asia and South Pacific Design Automation Conference (ASP-DAC)*, January 2004.

18. <u>M. Reshadi</u>, N. Dutt, "**Reducing Compilation Time Overhead in Compiled Simulators**", *International Conference on Computer Design (ICCD)*, October 2003.

19. <u>M. Reshadi</u>, N. Bansal, P. Mishra, N. Dutt, "**An Efficient Retargetable Framework for Instruction-Set Simulation**", *International Symposium on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, October 2003. **Best Paper Award.**

20. <u>M. Reshadi</u>, P. Mishra, N. Dutt, "**Instruction Set Compiled Simulation: A Technique for Fast and Flexible Instruction Set Simulation**", *Design Automation Conference (DAC)*, June 2003.

21. S. Gupta, <u>M. Reshadi</u>, N. Savoiu, N. Dutt, R.K. Gupta, A. Nicolau, "**Dynamic Common Sub-Expression Elimination during Scheduling in High-Level Synthesis**", *International Symposium on System Synthesis (ISSS)*, October 2002.

22. D. Rahmati, A. Salimi, <u>M. Reshadi</u>, Z. Navabi, "**Handling Complex VHDL Semantics with an OO Intermediate Format**", *IEEE Canadian Conference on Electrical & Computer Engineering (CCECE)*, May 2001.

23. B. Gorjiara, <u>M. Reshadi</u>, M. Fakhraie, "**GeReDiF: Using XML as a Structured Data Format in Grid Applications**", *IEEE International Symposium on Cluster Computing and the Grid (CCGrid)*, May 2001.

24. <u>M. Reshadi</u>, B. Gorji-Ara, Z. Navabi, "**Portability and Security, All in CHIRE File System**", *Hardware Description Language Conference (HDLCon)*, February 2001.

25. <u>M. Reshadi</u>, A. M. Gharehbaghi, Z. Navabi, "**AIRE/CE: A Revision Towards CAD Tool Integration**", *International Conference on Microelectronics (ICM)*, November 2000.

26. <u>M. Reshadi</u>, B. Gorji-Ara, Z.Navabi, "**HDML: Compiled VHDL in XML**", *VHDL International Users Forum (VIUF)*, October 2000.

27. <u>M. Reshadi</u>, A. M. Gharehbaghi, Z. Navabi, "**Intermediate Format Standardization: Ambiguities, Deficiencies, Portability issues, Documentation and Improvements**", *Hardware Description Language Conference (HDLCon)*, March 2000.

Technical Reports (available at Center for Embedded Computer Systems website: http://www.cecs.uci.edu)

1. B. Gorjiara, <u>M. Reshadi</u>, D. Gajski, "**NISC Communication Interface**", TR 06-05, March 2006.
2. <u>M. Reshadi</u>, B. Gorjiara, D. Gajski, "**NISC Technology and Preliminary Results**", TR 05-11, August 2005.
3. <u>M. Reshadi</u>, D. Gajski, "**NISC Modeling and Compilation**", TR 04-33, December 2004.
4. D. Gajski, <u>M. Reshadi</u>, "**NISC Application and Advantages**", TR 04-12, May 2004.
5. <u>M. Reshadi</u>, D. Gajski, "**NISC Modeling and Simulation**", TR 04-08, March 2004.
6. <u>M. Reshadi</u>, N. Dutt, "**RCPN: Reduced Colored Petri Nets for Efficient Modeling of Pipelined Processors and Generation of Very Fast Cycle-Accurate Simulators**", TR 03-48, December 2003.
7. B. Gorjiara, F. Kuester, P. Chou, <u>M. Reshadi</u>, "**GX-GUI: A General Extensible Technique for 2-D Interaction with VR Applications**", TR 03-46, January 2003.
8. <u>M. Reshadi</u>, P. Mishra, N. Bansal, N. Dutt, "**ReXsim: A Retargetable Framework for Instruction-Set Architecture Simulation**", TR 03-05, February 2003.

Research Experience

Graduate Research Assistant   **01/ 2004 – 12/2007**

Embedded Systems Methodology Group, University of California, Irvine.

- Developed new No-Instruction-Set-Computer (NISC) technology for designing custom (application specific) processors or dedicated hardware accelerators.
- Developed new compiler technology (~50,000 lines of C++ code) that combines traditional compiler techniques with High-Level Synthesis algorithms. The developed compiler accepts programs written in ANSI C or a subset of CIL assembly in .NET.
- Developed a new scheduling algorithm for the compiler that efficiently supports operation chaining, multi-cycle components, and non-uniform pipelined datapaths.
- Participated in development of the specification format for modeling a NISC processor as well as modeling a system consisting of multiple NISC processors.
- Participated in development of a framework that integrates different NISC tools. It gets the model of a NISC processor plus the program C code or .NET assembly and generates different outputs including simulatable and synthesizable Verilog RTL of the whole system as well as different views of the status of pipeline used for debugging and evaluation of the results.
- Developed a web-based interface for the NISC tool-set framework available at http://www.cecs.uci.edu/~nisc.

Graduate Research Assistant   **09/ 2001 – 12/2004**

Architecture and Compilers for Embedded Systems Group, University of California, Irvine.

- Researched high-performance retargetable techniques for cycle-accurate simulation
  Developed *Reduced Colored Petri Net* (*RCPN*) a very generic and intuitive formalism for modeling complex pipelined processors and generating very high performance cycle-accurate simulators.
  Developed cycle-accurate simulators for *StrongArm* and *XScale* processors using RCPN. The generated simulator runs 15 times on average faster than the very popular *SimpleScalar* simulator for ARM.
- Researched high-performance retargetable techniques for instruction-set simulation
  Developed a concise template-based formalism for modeling instruction-set of processors and generating high performance instruction-set simulator.
  Developed a new hybrid simulation technique that combined interpretive and compiled simulation algorithms.

Developed algorithms for: (a) compilation-time reduction, (b) general instruction-binary decoding, (c) and fast instruction execution utilizing partial evaluation and memory-access time reduction.

Developed instruction-set simulators for *ARM* and *SPARC* processors.

- Researched course-grained reconfigurable array processors and design exploration tool requirements for such architectures. Developed models for analyzing the performance of a reconfigurable matrix of processing elements as a co-processor for a general-purpose processor.
- Implemented several compiler analysis and optimizations in the SPARK High-Level Synthesis framework.

Graduate Research Assistant   10/ 1998 – 03/2001

CAD Lab, University of Tehran, Iran.

- Developed an extensible, platform-independent intermediate format for hardware description languages (HDLs) specifically VDHL and designed an integrated multi-format (Binary, XML, formatted text) file representations for it. The format was then used in other tools such as VHDL Compiler and VHDL Simulator in the group.
- Developed several logic synthesis algorithms for converting the intermediate format to Boolean expressions and eventually gates.
- Participated in the design and development of a compiled simulation of VHDL language.
- Initiated and supervised development of a generic Graphical Schematic Editor used for designing logic circuits.
- Initiated and supervised development of a generic Integrated Development Environment (IDE) used for integrating several tools that were developed in the CAD Lab by different researchers.
- Coordinated the Simulation, Compiler and Synthesis groups in the CAD lab.
- Implemented several fault tolerant architectural techniques in behavioral and structural VHDL.